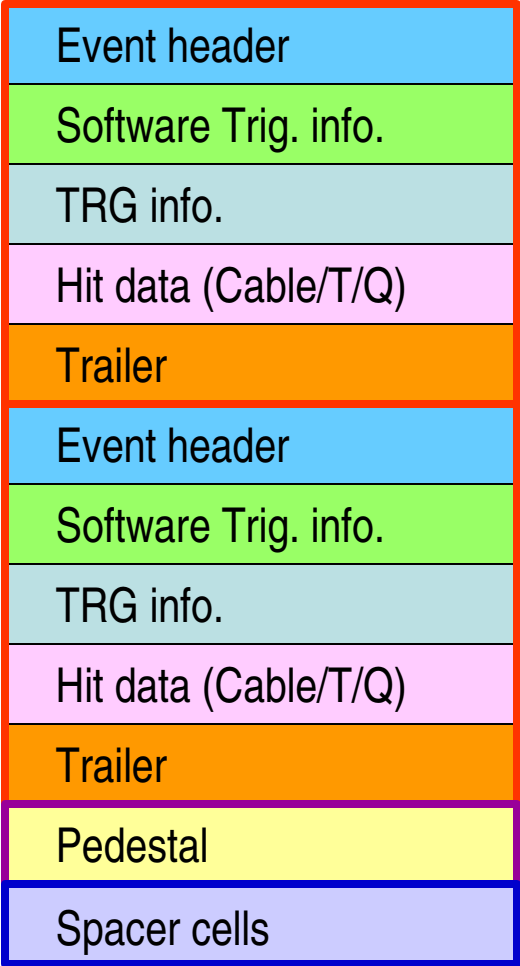


Online data format

2008 July 28

Data structure after the software trigger.



T/Q (16bits) from Sorter & Merger

| | |
|-------------------------|----------------------------------------------------------------|
| Header | |
| Length | In byte |
| ID (*) | 0xXXXX0001 : QBEE TQ Block |
| Host ID | ID of the readout computer (64bits) |
| Run # | Run # |
| Counter1 | 32bit Trigger counter |
| N/A 1 | N/A 1 |
| N/A 2 | N/A 2 |
| Counter2 | Lower 12 bits of the counter (**) |
| Contents | Contents of this data block (***) |
| Loc. hits | Starting point of the hit data |
| Len. hits | Length of the hit data |
| FIFO Full | (Only if exists) |
| Error cell (64bits) | 16bits additional information. + 48bits Data cell from ATM. |
| Hit data | |
| Data | C/T/Q (48bit C+T+Q per hit) |

T/Q from ATM sorted in the order of timing

(*) Incomplete: some hits might be missing because of FIFO FULL.

Corrupted : Corrupted data

If there are corrupted data in an event, this event is tagged as CORRUPTED.

(**) 12bit Trigger counter which comes with each T/Q hit data.

(***) Indicates what kind of data is included in this event buffer.

0x0001 : Normal

0x00100000: Incomplete T/Q

0x00200000: Corrupted T/Q

0x00400000: TRG mismatched T/Q

0x00800000: Corrupted ADC

T/Q (16bits) from Sorter & Merger

T/Q from ATM sorted in the order of timing

C/T/Q format (for usual hits)

| | | | | |
|------------------|----------|-----------------------------|------------------|--|
| 0 | 0 | Cable number (1 ~ 22000?) | | |
| Range | Trig. ID | IG | ADC count [10:0] | |
| TDC count [15:0] | | | | |

IG : In gate (In the software event gate) flag

Range : Charge range

Trig. ID : Normal hits or hits in the pedestal event

DB FIFO Nearly FULL

| | | | | |
|------------------|---|----------------|------------------|------------|
| 0 | 1 | Host ID | ATM ID | |
| Header (1111) | | Type (0001) | Status (1000) | SeqNo[3:0] |
| Reserved | | | | |
| Reserved | | | | |

Pedestal data

| | |
|-------------------|-------------------------------------|
| Header | |
| Length | In byte |
| ID (*) | 0x00000040 : Pedestal histo. block |
| Host ID | ID of the readout computer (64bits) |
| Run # | Run # |
| Counter1 | 32bit Trigger counter |
| N/A 1 | N/A 1 |
| N/A 2 | N/A 2 |
| First ctr. | First HW counter (32bit) |
| Last ctr. | Last HW counter (32bit) |
| qbcfg loc. | Index of the QBEE configuration |
| calcfg loc. | Index of the CAL configuration |
| qtccfg loc. | Index of the QTC configuration |
| ped loc. | Index of the pedestal histogram |
| caltbl loc. | Index of the CAL data. |
| QB Conf. | |
| CAL Conf. | |
| QTC conf. | |
| Pedestal | |
| CAL. table | |

This data block is used

to send pedestal data

calculated by SORTER

Pedestal events are recorded at ?Hz.

(Need to accumulate ~ 100events?)

(*) The ID for the pedestal histogram is

0x00000040

But the pedestal start

0x00000010

and the pedestal end

0x00000080

might be set at the same time.

Pedestal data

| QB cfg. | |
|------------|---------------------------|
| Address | Module Address (16bits) |
| Header (*) | Elec. header info |
| Serial id | Module serial number |
| Temp. | Temperature |

| CAL cfg. | |
|-------------|---------------------------|
| Address | Module Address (16bits) |
| Header (**) | Elec. header info |
| DAC volt. | DAC setting |
| CTR + gain | Gain + Counter (***) |

| QTC cfg. | |
|--------------|-------------------------------|
| Address | Module Address (16bits) |
| Header(****) | Elec. header info |
| Param. 1 | Discriminator thr. + Gain (+) |
| Param. 2 | I3 + COMP1 (++) |

(*) Header is defined as follows

1100101000XXXXXX

the lowest 6 bits gives the status info.

(**) Header is defined as follows

1110100001000000

(***) Counter + Gain is defined as follows

XXYYZZZZZZZZZZZZZZ

X 2 bits : N/A

Y 2 bits : Gain

Z 12 bits : HW CTR (lower 12 bits)

(****) Header is defined as follows

111000XXXXYYYYYYYY

X 4 bits : QTC-No.(0-7)

Y 6 bits : Status

(+) Discriminator thr. + Gain

XX00YYZZWWWWWWWWW

X 2 bits : QTC ch# (0-2)

Y 2 bits: sub ch(0 small 1 midium 2 large)

Z 2 bits : Gain

Y 8 bits : Discriminator threshold

(++) I3 + COMP1

0XXYYYYYYYZZZZZZ

X 3bits : preamp-gain

Y 6 bits : I3

Y 6 bits : COMP1

Pedestal data

| Pedestal | |
|-----------------|----------------------------------|
| Data | Pedestal data (Cable) |
| Data | Pedestal data (T sigma / T mean) |
| Data | Pedestal data (Q sigma / Q mean) |
| Data | Pedestal data (T sigma / T mean) |
| Data | Pedestal data (Q sigma / Q mean) |
| Data | Pedestal data (T sigma / T mean) |
| Data | Pedestal data (Q sigma / Q mean) |
| Data | Pedestal data (Cable) |
| Data | Pedestal data (T sigma/ T mean) |

Each channel has 3 ranges
32bits/each sigma + mean

Tsigma (12bit) **Qsigma (16bit)**
Tmean (20bit) **Qmean (16bit)**

| CAL table | |
|------------------|-------------------------------------|
| Data | Calibration data (Cable) |
| Data | Calibration data (T sigma / T mean) |
| Data | Calibration data (Q sigma / Q mean) |
| Data | Calibration data (T sigma / T mean) |
| Data | Calibration data (Q sigma / Q mean) |
| Data | Calibration data (T sigma / T mean) |
| Data | Calibration data (Q sigma / Q mean) |
| Data | Calibration data (Cable) |
| Data | Calibration data (T sigma/ T mean) |

Each channel has 3 ranges
32bits/each sigma + mean

Tsigma (12bit) **Qsigma (16bit)**
Tmean (20bit) **Qmean (16bit)**

Spacer

Inserted every 64 events in the ATM.

Used to extend HW trigger counter from 12 to 31 bits. Also used to identify “missing” ATMs.

| Header | |
|--------------------|-------------------------------------|
| Length | In byte |
| ID | 0x00080000 : SPACER Block |
| Host ID | ID of the readout computer (64bits) |
| Run # | Run # |
| Counter1 | 32bit Trigger counter (**) |
| N/A 1 | N/A 1 |
| N/A 2 | N/A 2 |
| N/A 3 | N/A 3 |
| Contents | Contents of this data block |
| Spacer | |
| Data (64bits) | Spacer status from ATM 1(*) |
| Data | Spacer status from ATM 2 |
| Data | : |
| Data | Spacer status from ATM 30 |

(*) Format

| | | | | | | | | | | | |
|------------------------------------|---|---------|--|--|--|--|--|---------------|--|--|--|
| 1 | 0 | Host ID | | | | | | ATM ID | | | |
| | | | | | | | | Data ID 8bits | | | |
| Checksum (from spacer cell) [15:0] | | | | | | | | | | | |
| Checksum (calculated) [15:0] | | | | | | | | | | | |

(**) Trigger counter in the spacer cell is [31:4].

Therefore, lower 4 bits are always 0.

DB status flags (SDS Start/Completed, DB FIFO FULL)

Inserted when SDS started or completed by the daughter board

(SDS start / completed).

Inserted when the daughter board FIFO gets full (DB FIFO FULL).

| Header | |
|--------------|-------------------------------------|
| Length | In byte |
| ID | 0x00000004 : Status block |
| Host ID | ID of the readout computer (64bits) |
| Run # | Run # |
| Counter1 | 32bit Trigger counter (**) |
| N/A 1 | N/A 1 |
| N/A 2 | N/A 2 |
| N/A 3 | N/A 3 |
| Contents | Contents of this data block |
| SDS Flag | |
| Data (64bit) | SDS Flags |
| Data | : |
| Data | SDS Flags |

SDS start

| 0 | 1 | Host ID | ATM ID |
|---------------|---|-------------|--------------------------|
| Header (1111) | | Type (0001) | Status (0001) SeqNo[3:0] |
| SeqNo[19:4] | | | |
| SeqNo[35:20] | | | |

SDS completed

| 0 | 1 | Host ID | ATM ID |
|-----------------------------------------|---|-------------|--------------------------|
| Header (1111) | | Type (0001) | Status (0010) SeqNo[3:0] |
| Word count for this SDS (upper 16 bits) | | | |
| Word count for this SDS (lower 16bits) | | | |

DB FIFO Nearly FULL

| 0 | 1 | Host ID | ATM ID |
|---------------|---|-------------|--------------------------|
| Header (1111) | | Type (0001) | Status (1000) SeqNo[3:0] |
| Reserved | | | |
| Reserved | | | |

ATM status flags

Various ATM status and information (configuration, temperature)
is transferred by using the status data cell.

| Header | |
|------------------|-------------------------------------|
| Length | In byte |
| ID | 0x00000004 : Status block |
| Host ID | ID of the readout computer (64bits) |
| Run # | Run # |
| Counter1 | 32bit Trigger counter (**) |
| N/A 1 | N/A 1 |
| N/A 2 | N/A 2 |
| N/A 3 | N/A 3 |
| Contents | Contents of this data block |
| ATM stat. | |
| Data (64bit) | ATM status cell from ATM J |
| Data | ATM status cell from ATM K |
| Data | : |

AMT status cell

| 0 | 1 | Host ID | | ATM ID | |
|----------------------|---|---------|------------|--------|--------------|
| Header (1110) | | Cls. | Device No. | | Status Addr. |
| Status value [31:16] | | | | | |
| Status value [15:0] | | | | | |

Hardware TRG

data from TRG module

Hardware trigger number, trigger ID, 48bit clock.

| Header | |
|-------------------|-------------------------------------|
| Length | In byte |
| ID | 0x00000002 : HW TRG block |
| Host ID | ID of the readout computer (64bits) |
| Run # | Run # |
| Counter1 | 32bit Trigger counter (**) |
| N/A 1 | N/A 1 |
| N/A 2 | N/A 2 |
| TRG | |
| Data (224bits) | TRG data cell |

TRG data cell (7 * 32 bits)

| |
|----------------------|
| Unix time |
| N/A 2 |
| Trigger counter |
| HW Trigger ID [15:0] |
| 48bit CLK [47:32] |
| 48bit CLK [31:16] |
| 48bit CLK [15:0] |

Software TRG

| | |
|-------------------|-------------------------------------|
| Header | |
| Length | In byte |
| ID | 0x80000000 : SW TRG block |
| Host ID | ID of the readout computer (64bits) |
| Run # | Run # |
| Counter1 | 32bit Trigger counter (**) |
| N/A 1 | N/A 1 |
| N/A 2 | N/A 2 |
| Soft Trig. | |
| N/A | |
| Trg mask | Trigger mask |
| Event # | 32bit (software trigger tentative) |
| Trig. ID | Trigger ID (32bit by software) |
| Trig. ver. | Trigger version / Trig. CPU ID |
| T0 | Initial timing (in TDC count) |
| g.width | Gate width |
| nhits | Number of hits (for triggering) |
| NTRG | Number of HW trig. included |
| CLK48 | 48bit clock (3 x 32 bits) |

GPS

data from GPS system (SK & T2K)

| Header | |
|--------------------|----------------------------|
| Length | In byte |
| ID | 0x00000800 : GPS (SK) data |
| Host ID (64bit) | ID of the readout computer |
| Counter1 | 31bit Trigger counter |
| N/A | Reserved |
| N/A | Reserved |
| GPS | |
| Data (?? bits) | GPS data cell |

GPS data cell

```
unsigned int    counter_32;
unsigned int    NA2;
unsigned int    av_freq;
unsigned int    gpstime1[2];
unsigned int    gpstime2[2];
unsigned int    ltgps1[2];
unsigned int    ltgps2[2];
unsigned int    ltctr[2];
unsigned int    cputime;
unsigned int    status;
struct timespec gps1;
/*
    struct timespec
    {
        __time_t tv_sec;
        long int tv_nsec;
    };
*/
unsigned int    ltccorr;
struct timespec gps2;
unsigned int    diffutc;
struct timespec utc1;
struct timespec utc2;
```

Raw AMT hits

This data block is used to raw AMT data for the debugging purpose.

| Header | |
|---------------------|----------------------------|
| Length | In byte |
| ID | 0x00000400 : Raw AMT DATA |
| Host ID (64bits) | ID of the readout computer |
| Counter1 | 31bit Trigger counter |
| Counter2 | 12bit Trigger counter (*) |
| N/A | Reserved |
| Raw AMT | |
| Data (48 bits) | AMT raw data |
| Data | : |
| Data | : |

(*) 12bit Trigger counter which comes with each T/Q hit data.

Raw AMT hit cell

| 0 | 1 | Host ID | ATM ID |
|---------------------------|---|---------|----------|
| Header (1101) | | TDC ID | Reserved |
| Raw data from AMT [31:16] | | | |
| Raw data from AMT [15:0] | | | |

Mismatched event counter T/Q (16bits) from Sorter & Merger

T/Q from ATM sorted in the order of timing

C/T/Q format (for mismatched events)

| | | | |
|------------------|-----|-----------------------|--------|
| 0 | 1 | Host ID | ATM ID |
| Channel # | | ADC count [10:0] | |
| RNG | TRG | Trigger counter[11:0] | |
| TDC count [15:0] | | | |

DB FIFO Nearly FULL

| | | | | |
|------------------|---|----------------|------------------|------------|
| 0 | 1 | Host ID | ATM ID | |
| Header (1111) | | Type (0001) | Status (1000) | SeqNo[3:0] |
| Reserved | | | | |
| Reserved | | | | |

Global data structure in the online programs

Data structure from Collector to Sorter

Inserted every 64 events

| |
|----------------------------------|
| Spacer |
| Hit data cell (T/Q) |
| Hit data cell (T/Q) |
| : |
| Hit data cell (T/Q) |
| Spacer |
| Hit data cell (T/Q) |
| Hit data cell (T/Q) |
| Hit data cell (pedestal T/Q) |
| Hit data cell (pedestal T/Q) |
| Status cell (temperature etc.) |
| Hit data cell (T/Q) |
| FIFO FULL |
| Hit data cell (T/Q) |
| Spacer |
| Hit data cell (T/Q) |



| |
|----------------------------------|
| Header |
| Spacer |
| Hit data cell (T/Q) |
| Hit data cell (T/Q) |
| : |
| Hit data cell (T/Q) |
| Trailer |
| Header |
| Spacer |
| Hit data cell (T/Q) |
| : |
| Hit data cell (pedestal T/Q) |
| Hit data cell (pedestal T/Q) |
| Status cell (temperature etc.) |
| Hit data cell (T/Q) |
| FIFO FULL |
| Hit data cell (T/Q) |
| Trailer |
| Header |
| Spacer |
| Hit data cell (T/Q) |

