

Electronics Lab Manual

Laboratory 9.1	Digital Circuits
Name	Section

PURPOSE

1. Observe the operation of a NAND gate.
2. Design and build a circuit to produce the magnitude of 3-bit number.
3. Design and build a circuit to take the two's complement of a 3-bit number.

COMMENTS

Digital circuit elements are easily damaged by rough handling and overvoltages. Before you come to lab, read the digital circuits section in the preface to this manual.

SPECIAL EQUIPMENT

Several TTL chips are used in this lab: a minimum set would include inverters, NANDS, NORs, and an XOR. The work requires fewer wires if AND and OR functions are also available. The 74LS00 family of chips is recommended. Also needed are three LEDs, three switches in a dual inline package (DIP), and two toggle switches or push-buttons. (Note: The push-buttons on the Global Specialties PB-503 breadboard are really the open-collectors of transistors that have their emitters connected to ground. The NO outputs work as needed in Section A.)

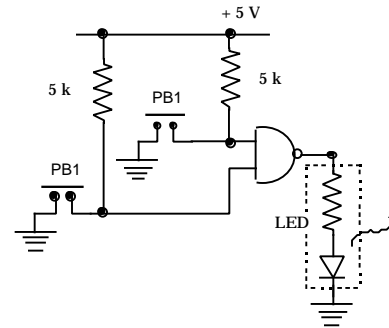
A. NAND Gate Operation

1. Build the circuit.

- a. The following test circuit will allow you to exercise the NAND gate by applying all of the four possible inputs. Note that the current direction is out of the TTL inputs, probably contrary to your initial expectations (see Fig. 9.20).

Check with your instructor to see if you need to insert current limiting resistors in series with your LEDs: the PB-503 breadboard does not require them. The pushbuttons on this breadboard have an internal connection to ground and the NO outputs function as indicated on this schematic.

- b. From your observations of this circuit, complete the truth table for this operation.



PB1	PB2	LED
up	up	
up	down	
down	up	
down	down	

B. Magnitude of Two's Complement Number

1. Preliminary design work

Do the work in Section 1 before you come to lab.

In this part you will use three lines of a DIP switch to form an input number *ABC*. Connect one side of each switch to ground (a slide switch on the PB-503), and pull up each input with a 5 k resistor to +5 volts, just like the pushbuttons in Section A.

The three switches form a three-bit input number *ABC* which in two's complement notation can define any number from -4 to +3.

- a. Complete the truth table for a two-bit output number *DE* that defines the magnitude of the *ABC* number in the -3 to +3 range. You can ignore the -4 state: we will assume that this input state never occurs.
- b. Write logic equations for the true states of the *D* and *E* output variables, then reduce until these two functions can be mechanized with one XOR and four additional NAND gates. (You may want start with a Karnaugh map. You have one "don't care" state which can be set to one. An application of DeMorgan's theorem will then get the result into the NAND gate form.)

	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>	<i>E</i>
0	0	0	0		
1	0	0	1		
2	0	1	0		
3	0	1	1		
-4	1	0	0		
-3	1	0	1		
-2	1	1	0		
-1	1	1	1		

- c. Draw the circuit using NAND and XOR logic symbols and pin numbers from the package outlines.

2. Build this circuit

Use two LEDs to show the output state, then test the circuit for various switch settings.

C. Complement of 3-bit Number

1. Preliminary design work

Do the work in this section before you come to lab.

- a. The two's complement of a number is formed by complementing the number bit by bit, then adding one to the result, dropping any overflow beyond the original number of bits. If ABC is the 3-bit number then its two's complement DEF is given by

$$\begin{array}{r} \bar{A} \bar{B} \bar{C} \\ + \quad 1 \\ \hline D E F \end{array}$$

Complete the truth table at the right so it describes this operation.

	A	B	C	D	E	F
0	0	0	0			
1	0	0	1			
2	0	1	0			
3	0	1	1			
-4	1	0	0			
-3	1	0	1			
-2	1	1	0			
-1	1	1	1			

b. From the truth table, write a minterm logic equation for the true state of each of these output variables, then reduce these equations as much as possible. You should take advantage of a recurring exclusive-OR combination.

c. Mechanize these three equations using INVERT, AND, OR, and XOR functions. Omit pin numbers from this drawing.

2. Build this circuit.

a. Redraw the circuit if necessary to use logic elements available in lab. Identify each logic element with a chip location and pin numbers.

